AMENDMENTS TO THE CLAIMS

Please cancel claim 14 without prejudice or disclaimer of its underlying subject matter.

Please amend the claims as follows.

1. (original) A digital signal processing device comprising:

multiplication means for multiplying an input ΔΣ modulation signal generated from ΔΣ modulation by a factor;

ΔΣ modulation means having a plurality of integrators for varying effective orders and applying ΔΣ modulation again to an output from said multiplication means; and

switchover means for switching between a reprocessed ΔΣ modulation signal from said ΔΣ modulation means and said input ΔΣ modulation signal.

2. (original) The digital signal processing device according to claim 1, wherein said ΔΣ modulation means comprises order control means for varying effective orders depending on signal switchover situations in said switchover means.

3. (previously presented) The digital signal processing device according to claim 2, wherein said order control means varies effective orders for said ΔΣ modulation means at an

approximate timing when said switchover means switches between said input ΔΣ modulation signal and said reprocessed ΔΣ modulation signal.

4. (original) The digital signal processing device according to claim 2, wherein said order control means varies effective orders for said ΔΣ modulation means at an approximate timing when said switchover means switches between a fixed signal changing to no sound in an audible band and music data processed with ΔΣ modulation.

5. (original) The digital signal processing device according to claim 1, wherein said ΔΣ modulation means comprises fraction elimination means for eliminating a fraction remaining in said integrator.

6. (original) A digital signal processing method, comprising steps of:

a multiplication step for multiplying an input ΔΣ modulation signal generated from ΔΣ modulation by a specified factor for specified processing;

a reprocessed ΔΣ modulation step for reapplying ΔΣ modulation to an output provided with said specified processing by using a ΔΣ modulator comprising a plurality of integrators for varying effective orders; and

a switchover step for switching between said input ΔΣ modulation signal and said reprocessed ΔΣ modulation signal.

7. (original) The digital signal processing method according to claim 6, wherein said reprocessed ΔΣ modulation step varies effective orders for said ΔΣ modulator depending on signal switchover situations in said switchover step.

8. (original) The digital signal processing method according to claim 7, wherein said reprocessed ΔΣ modulation step varies effective orders for said ΔΣ modulator at an approximate timing when said switchover step switches between said input ΔΣ modulation signal and said reprocessed ΔΣ modulation signal.

9. (original) The digital signal processing method according to claim 7, wherein said reprocessed ΔΣ modulation step varies effective orders for said ΔΣ modulator at an approximate timing when said switchover step switches between a fixed signal changing to no sound in an audible band and music data processed with ΔΣ modulation.

10. (original) The digital signal processing method according to claim 6, wherein said reprocessed ΔΣ modulation step not only varies effective orders for a ΔΣ modulator, but also eliminates a fraction remaining in said integrator.

11. (canceled)

12. (currently amended) A ΔΣ modulator for applying ΔΣ modulation to a multi-bit signal comprising:

an integrator of a plurality of ~~said~~ integrators having fraction elimination means for eliminating a fraction remaining in said integrator, and

order variation means for varying effective orders increasing due to connection with said plurality of said integrators,

wherein said integrator further includes:

an integrator adder that receives an output from said fraction elimination means; and

an integrator delay circuit that delays an output from said integrator adder, said delayed output from said integrator adder being provided to said fraction elimination means.

13. (previously presented) The ΔΣ modulator according to claim 12, wherein said fraction is data smaller than or equal to 1.

14. (canceled).

15. (previously presented) The ΔΣ modulator according to claim 12, wherein said ΔΣ modulator receives an input, an effective order of said effective orders being the number of said integrators participating in the modulation of said input.

16. (currently amended) The ΔΣ modulator according to claim 15, further comprising:

a first multiplier, a first control factor supplied from said order variation means being received by said first multiplier to generate a first multiplication output, said first multiplier multiplying said input by said first control factor to generate said first multiplication output;

a second multiplier, a second control factor supplied from said order variation means being received by ~~first~~ said second multiplier to generate a second multiplication output, said second multiplier multiplying an output from another integrator of said plurality of said integrators by said second control factor to generate said second multiplication output.

17. (previously presented) The ΔΣ modulator according to claim 16, further comprising:

a first adder that generates a first addition output by adding said input and quantized data from a quantizer.

18. (previously presented) The ΔΣ modulator according to claim 17, wherein said another integrator receives said first addition output.

19. (previously presented) The ΔΣ modulator according to claim 16, further comprising:

a level adjuster that multiplies said second multiplication output by a gain to generate a level adjustment; and

an second adder that generates a second addition output by adding said first multiplication output, said level adjustment, and quantized data from a quantizer.

20. (previously presented) The ΔΣ modulator according to claim 19, wherein said integrator receives said second addition output.

21. (previously presented) The ΔΣ modulator according to claim 16, wherein:

(said first control factor) = 1.0 – (said second control factor).

22. (previously presented) The ΔΣ modulator according to claim 21, wherein said first control factor is "0.0" when said number of said integrators equals said plurality of said integrators.

23. (previously presented) The ΔΣ modulator according to claim 21, wherein said first control factor is "0.1" when said number of said integrators is less than said plurality of said integrators.